

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

nulla'

What is claimed is:

1. A manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

5 (a) forming said MISFET on the main surface of said semiconductor substrate;

(b) forming an insulating film above said MISFET by the plasma CVD method at a temperature of 450°C to 700°C;

10 (c) forming a trench by etching said insulating film; and

(d) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said insulating film to form a lower electrode of said capacitor on the inner wall of the trench.

15 2. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

20 wherein crystal grains grown from crystal nucleuses of silicon are formed on a surface of the silicon film of said step (d).

25 3. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said manufacturing method of a semiconductor integrated circuit device further comprises, after the step 25 (d), the steps of:

(e) forming a capacitor insulating film of said capacitor on said lower electrode; and

(f) forming a conductive film constituting an upper

~~electrode of said capacitor on said capacitor insulating film.~~

Mark 7
4. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

5. wherein said semiconductor integrated circuit device has an area in which said memory cell is formed and an area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

10. (e) forming, in said area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

15. 5. The manufacturing method of a semiconductor integrated circuit device according to claim 1,

wherein said plasma CVD method is the CVD method using a high-density plasma.

6. 6. A manufacturing method of a semiconductor integrated circuit device comprising a memory cell formed of a MISFET and a capacitor formed on a main surface of a semiconductor substrate, said method comprising the steps of:

(a) forming said MISFET on the main surface of said semiconductor substrate;

25. (b) depositing a first insulating film above said MISFET at a predetermined temperature;

(c) depositing a second insulating film on said first insulating film at a temperature higher than said

predetermined temperature;

(d) forming a trench by etching said first and second insulating films; and

5 (e) depositing a silicon film on said insulating film and in said trench, and removing the silicon film on said second insulating film to form a lower electrode of said capacitor on the inner wall of the trench.

7. The manufacturing method of a semiconductor integrated circuit device according to claim 6,

10 wherein said temperature higher than said predetermined temperature is in a range of 450°C to 700°C.

8. The manufacturing method of a semiconductor integrated circuit device according to claim 6,

15 wherein crystal grains grown from crystal nucleuses of silicon are formed on a surface of the silicon film of said step (e).

9. The manufacturing method of a semiconductor integrated circuit device according to claim 6,

20 wherein said manufacturing method of a semiconductor integrated circuit device further comprises, after the step (e), the steps of:

(f) forming a capacitor insulating film of said capacitor on said lower electrode; and

25 (g) forming a conductive film constituting an upper electrode of said capacitor on said capacitor insulating film.

10. The manufacturing method of a semiconductor integrated circuit device according to claim 6,

wherein said semiconductor integrated circuit device

M163

*mult 93
cancel*

has an area in which said memory cell is formed and an area in which a logic circuit is formed, and said manufacturing method of a semiconductor integrated circuit device comprises, before said step (b), the step of:

5 (f) forming, in said area in which a logic circuit is formed, an n channel MISFET and a p channel MISFET constituting said logic circuit, each of said n channel MISFET and said p channel MISFET comprising a gate electrode containing n type impurity and a gate electrode containing p type impurity, respectively.

10 11. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate; and

15 (b) forming an insulating film containing impurity above said MISFET by the plasma CVD method at a temperature of 450°C to 700°C.

12. The manufacturing method of a semiconductor integrated circuit device according to claim 11,

20 wherein said impurity is phosphorus.

13. ~~The manufacturing method of a semiconductor integrated circuit device according to claim 11,~~

wherein said plasma CVD method is the CVD method using a high-density plasma.

25 14. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a MISFET on a main surface of a semiconductor substrate,

(b) depositing a first insulating film above said MISFET at a predetermined temperature;

(c) planarizing a surface of said first insulating film; and

5 (d) forming a second insulating film containing impurity on said first insulating film at a temperature higher than said predetermined temperature.

15. The manufacturing method of a semiconductor integrated circuit device according to claim 14,

10 wherein said impurity is phosphorus.

16. The manufacturing method of a semiconductor integrated circuit device according to claim 14,

wherein said first and second insulating films are formed by the CVD method using high-density plasma.

15 17. A semiconductor integrated circuit device, comprising:

(a) a MISFET formed on a main surface of a semiconductor substrate; and

(b) a capacitor connected in series to said MISFET,

wherein said capacitor comprises:

20 (b1) a lower electrode made of a silicon film, which is formed at a concave portion in a lamination layer of a first insulating film formed above said MISFET and a second insulating film formed on said first insulating film and having smaller impurity content than said first insulating film;

(b2) a capacitor insulating film formed on said lower electrode; and

(b3) an upper electrode formed of a conductive film

formed on said capacitor insulating film.

18. A semiconductor integrated circuit device, comprising:

(a) a MISFET formed on a main surface of a semiconductor substrate; and

5 (b) a capacitor connected in series to said MISFET,

wherein said capacitor comprises:

(b1) a lower electrode made of a silicon film, which is formed at a concave portion in a lamination layer of a first insulating film formed above said MISFET and a second insulating film which is thinner than said first insulating film and formed on said first insulating film;

(b2) a capacitor insulating film formed on said lower electrode; and

(b3) an upper electrode formed of a conductive film formed on said capacitor insulating film.

19. The semiconductor integrated circuit device, according to claim 18,

wherein said second insulating film has a smaller impurity content than said first insulating film.